# Appendix L

# Title:
# Timeslot Assigner Receive V2.2.1

# 1 Introduction

## 1.1 Overview

The Timeslot Assigner Receive TSAR (macro name key: TR_) maps the incoming receive timeslots (maximal 32 ports x 32 timeslots = 1024 timeslots and for the M256F 28 ports x 24 timeslots = 672 timeslots)to logical channels and provides the channel relevant information to the protocol machine interface.

## 1.2 Features

- coordinates requests of 32 ports [M256F: 28ports] by built-in arbitration
- arbitration priority from low (port n = 0) to high (port n=31)
- channel programming by indirect access through TFPI (FPI Slave) Interface
- data output FIFO buffering for adjustment of further data processing
- programmable channel assignment per timeslot
- programmable mask per timeslot
- programmable timeslot inhibit flag per timeslot
- remote channelwise loop, one channel at a time (loop RD -> TSAR -> TSAT -> TD)
- remote portwise loop, one port at a time (loop RD --> TSAR --> TSAT --> TD)
- loop supported by a jitter attenuator, consisting of a 512 bit FIFO with slip function
- programmable "TMA1ST flag" (tmafirst flag) to identify the 'first' timeslot for TMA mode channels
- FPI target interface
- performance: SYSCLK up to 70 MHz
- number of gates:
- area:
- power consumption:
- full scan path
- RAM (Timeslot Assigner Receive Parameter Table: TARPT) built in selftest
- RAM (Timeslot Assigner Receive Loop Fifo: TARLPFIFO) built in selftest
- RAM (Timeslot Assigner Receive Data Fifo: TARFIFO) built in selftest

## 1.3 System Integration

The TSAR (macro name key: TR_) has four interfaces:

- one FPI Slave (TFPI) Bus
- parallel REQ/GNT interface to (R)XPI functions (accept incoming data and corresponding timeslot information)

- REQ/GNT interface to PMR functions (provides channel information and data to processing functions)
- alternate output for remote loop (for one channel or port at a time)

The TSAR receives the synchronized data and corresponding port and time slot information from the (R)XPI block. The incoming data is mapped to channel relevant information and finally provided to the protocol machine. Additionally this data can be selected for one single channel or port to provide the loop interface. Configuration of the TSAR is done via the FPI slave interface.

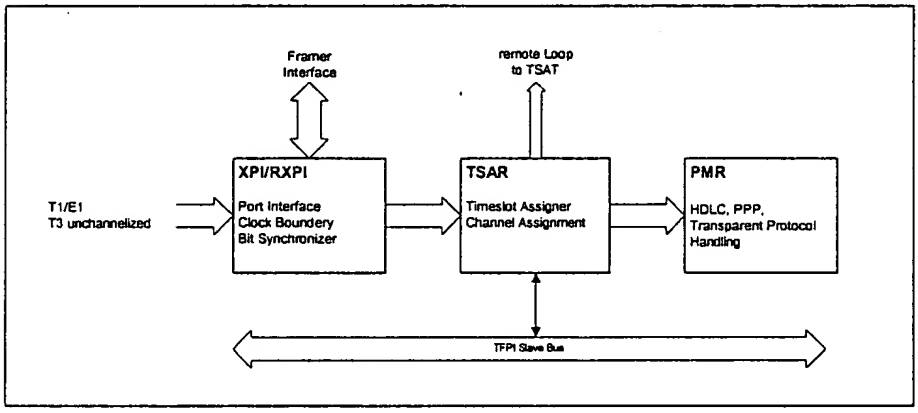



Figure 1.3:
**System integration**

## 1.4 Known Restrictions

1) necessary minimum SYSCLK to serve 32 ports at E1 data rate (32 timeslots), without regarding synchronization losses

one access request per timeslot; i.e. 2.048Mbit x 32 ports / 8bits/timeslot = 8 Mbyte/s and 4 clock cycles for processing (arbitration, mapping, data transfer) 33MHz SYSCLK would be sufficient.

in m256f application, i.e T1 1.544Mbit x 28ports / 8bits/timeslot = 5.4 Mbyte/s and 4 clock cycles for processing, the minimum frequency for SYSCLK = 22 MHz.

2) priority and waitstates for indirect read/write access from the FPI slave interface to the TARPT RAM.

For operation with maximum data rate, data processing takes every forth clock cycle access to the TARPT RAM. Else the TFPI slave interface has access to the TARPT. Thus an indirect write access can be delayed 1 clock cycle for write and 3 clock cycles for read.

3) restrictions regarding the remote loop:

a) Channelwise loop: same port for receive and transmit direction, same number of timeslots activated (inhibit bit = 0), identical mask bit field for all timeslots that are activated

b) Portwise loop: same port for receive and transmit direction, only one channel is supported which comprises all timeslots, inhibit bits are not allowed, identical mask bit field for all timeslots

4) timeslot to channel assignment programmed in the parameter table for unchannelized mode .

for unchannelized mode all timeslots of a port have to be assigned to one channel,. valid timeslots are timeslot 0 to 23.

## 2 Functional Description

### 2.1 Block Diagram

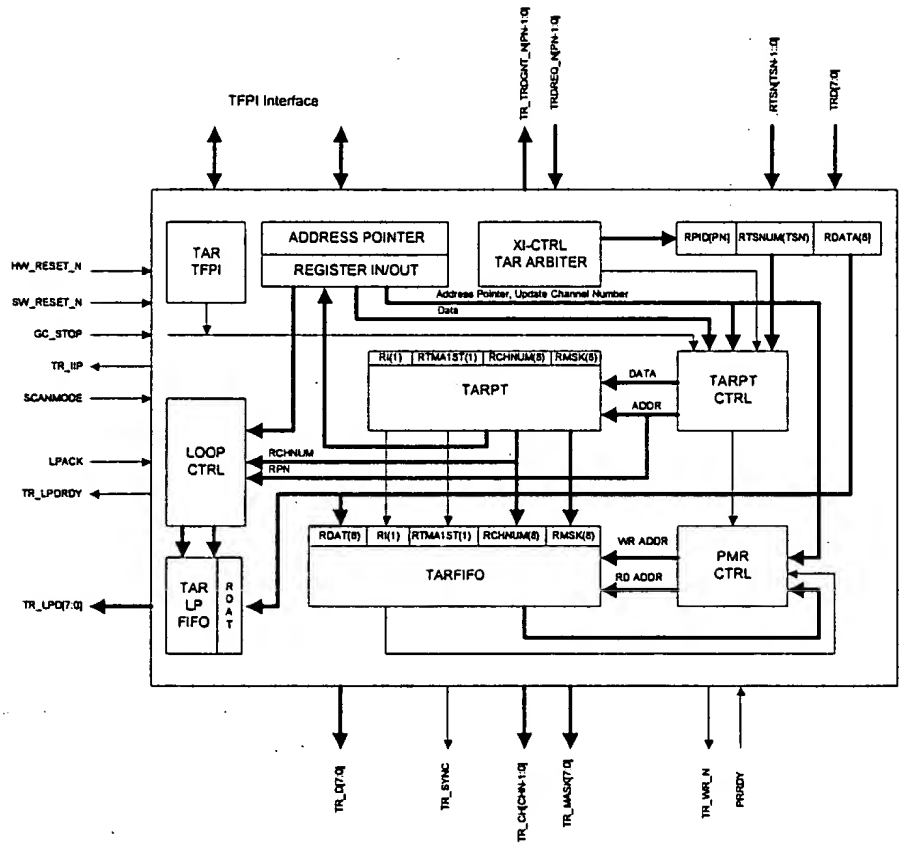



**Figure 2.1:**
**TSAR Block Diagram**

## 2.2 Normal Operation Description / Reset

With an active reset (HW_RESET_N or SW_RESET_N) all registers are set to their benign state and the TSARFIFO is reset to empty (there is no difference between HW and SW reset). After the reset signal has become inactive, the self initialization procedure in the TARPT RAM shell starts resetting the RAM values to RI = '1' (inhibit timeslot), TMA1ST = '0' (no TMA sync timeslot), CHNUM=00hex (channel number 0) and MASK = 00hex (all bits masked).

During this initialization period the TSAR is held in stop mode. The TSAR is inaccessible from all interfaces and doesn't generate any request itself. The active self init period is indicated by output TR_IIP = '1', which becomes '0', when the RAM TARPT is initialized.

For fast initialization of the TARPT RAM an input GC_STOP is still asserted (reset value) and keeps the TSAR in stop mode. In stop mode the contol logic assigns the TARPT access exclusively to the TFPI interface and normal operation to this RAM is suspended. Thus the initial programming of the TARPT can be achieved very fast since it is not interleaved by normal operation accesses. A request from the (R)XPI will be processed as in normal operation mode, but the timeslot and data information is discarded. The TARPT is programmed now by writing to the two TSAR indirect access registers. The TARPT address corresponds to the time slot number and port number.

In normal operation mode (GC_STOP='0') TFPI re-programming requests to TARPT are handled by the control logic as ordinary requests for access. Thus they can be delayed up to 1 clock cycles for write until the access is granted. For read cycles valid data is delayed 2 additional clock cycles because the access to the TARPT is pipelined. Before reprogramming a channel to timeslot mapping configuration the corresponding channel must be turned off in PMR, in order to avoid intermediate TARPT states for timeslots of that channel. The TARPT contains the following entries per time slot (address):

TARPT.RI (inhibit receive time slot)

TARPT.RTMA1ST (flag to be used by PMR)

TARPT.RCHNUM[7:0] (channel number for that timeslot)

TARPT.RMASK[7:0] (mask bits for that timeslot)

After deasserting the GC_STOP input signal, the TSAR is in normal operation mode. The arbiter now accepts requests from the TRDREQ_N signals and grants the data bus TRD and the time slot number bus RTSN to the selected initiator by asserting the corresponding TR_TRDGNT_N signal. After deasserting the corresponding TRDREQ_N signal (marks valid data on the busses) data is sampled for internal processing.

The following information is received from the (R)XPI:

requests for data processing from the (R)XPI : TRDREQ_N[PN-1:0]

timeslot number of granted (R)XPI : RTSN[4:0]

receive data of granted (R)XPI: TRD[7:0]

The timeslot number, which is received on RTSN bus is combined with the port ID, that the arbiter generates from the corresponding request line. The concatenation of timeslot number and port id points to a location in the TARPT. The corresponding contents is read and written into the TARFIFO. A transfer to PMR is started by TSAR by activating the request line TR_WR_N. In the same cycle the channel number and the mask lines are activated. For the first active timeslot of each logical channel in TMA mode, the TSAR activates the TR_SYNC line. This TMA1ST info flag is used in the protocol machine receive for synchronisation purposes to indicate the first timeslot in a frame, which is assigned to a multi-timeslot TMA channel. It must also be set for a single timeslot TMA channel. The data transaction is finished by PMR when the PRRDY line is active.

The following information is delivered to the PMR:

the receive data, which were received at TRD[7:0]: TR_D[7:0]

the assigned channel number: TR_CH[7:0]

the programmed mask for that timeslot: TR_MASK[7:0]

the TMA1ST info flag: TR_SYNC

### 2.3 Remote Loop

A basic channelwise or portwise remote loop is available from the TSAR to the TSAT. The payload of one (and only one) logical channel or port is mirrored from the receive part to the transmit part of the looped port. In SCM mode, the framing bits, CRC and spare bits are not looped. They are provided by the M256F framer and the facility data link controller. The channel number or port ID is programmed in the configuration register 2 CONF2. The loop is activated by setting the corresponding loop command bit in the configuration register 2 CONF2. Receive timeslots of that channel or port matching the programmed channel number or port ID are written to the TSAR loop FIFO (64 x 1 byte) which is implemented as a circularly organized memory controlled by a read pointer and a write pointer. The loop FIFO acts as a jitter attenuator which compensates the clock jitter between receive and transmit clock.

Only one loop command bit, either for channel or port loop, should be set at a time. Before programming the channel number or port ID, the loop must be turned off. Generally, the port number or channel number has to be programmed first before setting the portwise or channelwise loop command bit.

In case of a channel loop, the channel characteristics in receive and transmit direction must be identical. The numbers of active receive and transmit timeslots of the looped channel must be identical. The mask bit fields in the active timeslots must be identical.

In case of a port loop, only one channel is allowed which comprises all timeslots. Inhibit bits for the looped port are not allowed.

The data transfer for the looped channel or port to the PMR is not affected The loop is turned off by resetting the corresponding loop command bit. The LPDRDY signal is then deactivated, and the loop FIFO will be reset to empty.

Slip Function

After activating the loop, 32 receive data bytes are written to the loop FIFO until the LPDRDY signal is asserted by TSAR. TSAT then starts reading the transmit data from the loop FIFO. Hence, the initial distance between the FIFO read pointer (RP) and the write pointer (WP) is 32 bytes. Due to a RCLK/TCLK clock jitter the RP may move towards WP. In case the distance between RP and WP is equal plus/minus 1 byte a slip of the read pointer will occur. Provided RP is faster than WP a positive slip occurs (the previously received 31 bytes are read out twice). In case RP is slower than WP a negative slip occurs (the next 31 received bytes are skipped). The slip condition is checked with each access to the loop FIFO.

## 3 Macro Interfaces and Signal Description

All signals are active high until otherwise specified. Active low signals are designated by "_N" appended to their names. To make the design as re-usable as possible, a bus signal whose width is application dependent is specified with one of the following parameters:

| Parameter name | Bus Type | Typical Value (Bits) M256F |
|---|---|---|
| PN | max. port number bus | 5 |
| TSN | max. timeslot number bus | 5 |
| CHN | max. channel number bus | 8 |
| DB | data bus width | 32 |
| AB | address bus witdh | 30 |

### 3.1 Signal Description

#### 3.1.1 Global Signals

| Signal Name | Direction | Type | Tsu/ Thld Td | meaning/comment special characteristics |
|---|---|---|---|---|
| SYSCLK | i | | | internal system clock |
| HW_RESET_N<br>SW_RESET_N | i<br>i | | | general SW and HW Reset |
| SCANMODE | i | | | SCAN Test mode |
| GC_STOP | i | | | external init keeps TSAR in stop mode, exclusive access to TARPT RAM from TFPI |
| TR_IIP | o | | | TSAR initialization in progress following reset. TSAR is not availble when this signal is asserted. This signal will remain high for several clocks following release of TSAR reset(s). |

### 3.1.2 Receive Port Interface

The XPI(RXPI) interface consists of the following signals

| Signal Name | Direction | Type | Tsu/ Thld Td | meaning/comment special characteristics |
|---|---|---|---|---|
| TR_TRDGNT_N[PN-1:0] | o | | | data/tsnum bus is granted to receive port n=index |
| TRDREQ_N[PN-1:0] | i | | | request from receive port n=index for servicing/ reading 8 bit data |
| TRD[7:0] | i | | | data bus containing 8 bit serial/parallel converted time slot data (bit 0 is the first serial bit received, bit 7 is the last serial bit received) |
| RTSN[TSN-1:0] | i | | | time slot bus containing the time slot number of the corresponding data XI_TRD ( valid time slot numbers are 0 to 23 for T1, 0 to 31 for E1 **and for unchannelized mode all timeslots of a port have to be assigned to one channel** |

Description of the (R)XPI interface protocol:

As soon as any port RXPI[n] has 8 bit data available for processing, it asserts the signal TRDREQ_N to the arbiter part of the TSAR, in order to request service. The arbiter then grants by activating the respective grant signal TR_TRDGNT_N one port access to the busses TRD (data) and RTSN (time slot number). TRDREQ_N is deasserted to indicate valid data on the busses TRD and RTSN. TSAR reads the bus information and deasserts the TR_TRDGNT_N.

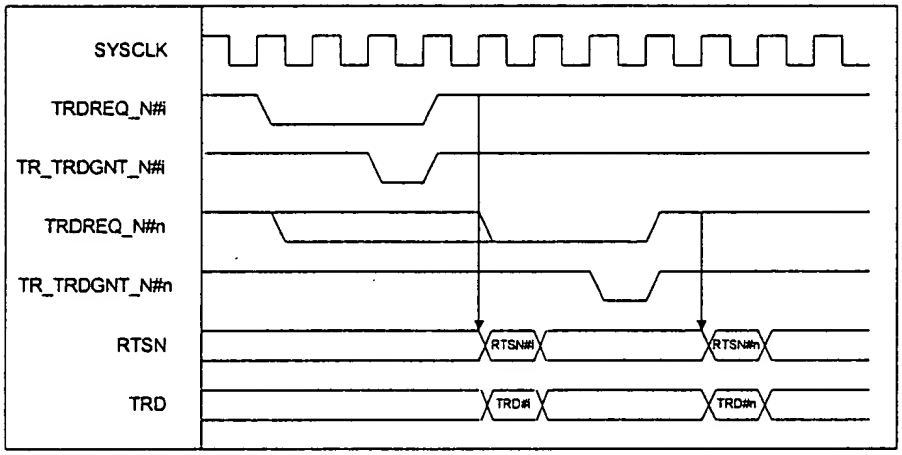



**Figure 3.1.2:**
**Data Transfer from XPI (RXPI) to TSAR**

### 3.1.3 Protocol Machine Receive Interface

The PMR interface consists of the following signals

| Signal Name | Direction | Type | Tsu/Thld Td | meaning/comment special characteristics |
|---|---|---|---|---|
| TR_WR_N | o | | | request for servicing/writing data |
| TR_D[7:0] | o | | | 8 bit data for PMR |
| TR_CH[CHN-1:0] | o | | | logical channel number |
| TR_MASK[7:0] | o | | | 8 bit mask field to enable single bits of TSA data |
| TR_SYNC | o | | | logical channel synchronization line in TMA mode |
| PRRDY | i | | | PMR finished data transaction |

Description of PMR interface protocol:

Whenever data in the TARFIFO is available a transfer is started by TSAR asserting the signal TR_WR_N. In the same cycle channel number, data and mask information is activated. For the first active timeslot of each logical channel in TMA mode, the TSAR

also actives the TR_SYNC line. The information is held stable until PMR finished data transaction by activating the line PRRDY.

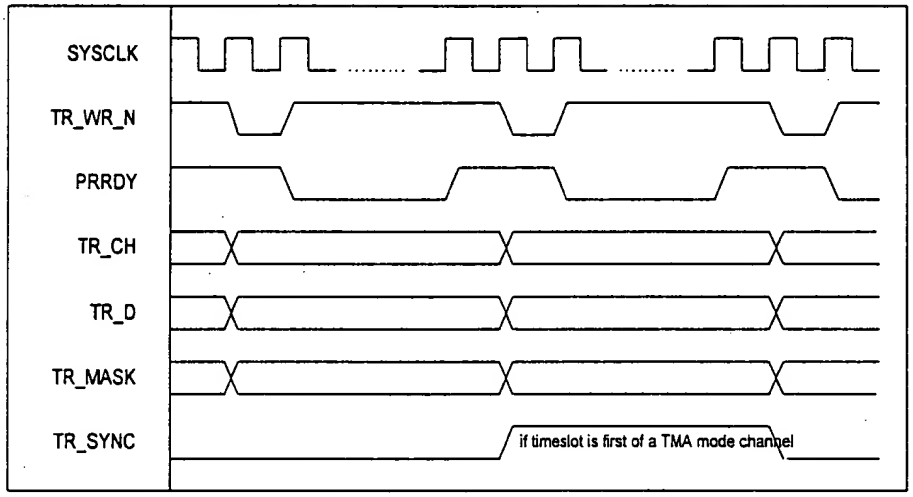



**Figure 3.1.3:**
**Data transfer from TSAR to PMR**

### 3.1.4 TSA Transmit Interface (for remote loop)

TheTSA transmit interface consists of the following signals

| Signal Name | Direction | Type | Tsu/ Thld Td | meaning/comment special characteristics |
|---|---|---|---|---|
| LPACK | i | | | acknowledge from TSAT data has been read |
| TR_LPD[7:0] | o | | | 8 bit timeslot data of channel or port which is in remote loop operation |
| TR_LPDRDY | o | | | indicates valid data available for loop operation |

Description of TSA transmit interface protocol:

The remote loop is activated by programming a remote loop with loop active flag set (CRLP or RLP). The corresponding timeslot data and mask bit field of the channel/port matching with programmed channel number (LPCN) or port ID (LPPID) is written into the

TAR LPFIFO. As soon as the LPFIFO is filled up, TR_LPDRDY signal is activated indicating valid data for the remote loop. The data is read out from the TAR LPFIFO by activating the signal LPACK. The remote loop is deactived by resetting the loop active flag.

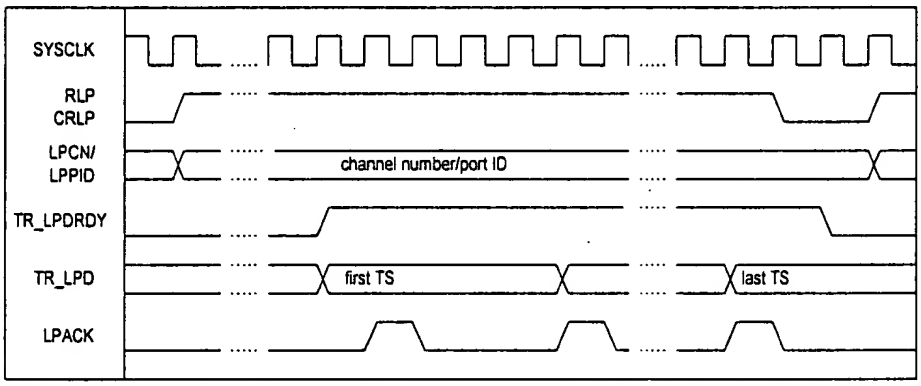



**Figure 3.1.4:**
**Data transfer on the loop interface**

### 3.1.5 FPI Slave Interface

In the following sections, "Flexible Peripheral Interconnect (FPI) Bus compliant" means that the specified bus uses a subset of the FPI features and satisfies the basic address and data cycle. Not all FPI signals are implemented because default values are sufficient for the application i.e. they can be coded as constants in the hardware. Refer to the FPI bus specification and FPI + Target Template Bus for details of the complete bus.

The TFPI interface consists of the following signals:

| Signal Name | Direction | Type | Tsu/ Thld Td | meaning/comment special characteristics |
|---|---|---|---|---|
| TFPI_RD_N | i | | | Read control input |
| TPFI_WR_N | i | | | Write control input |
| TFPI_A[AB-1:2] | i | | | Address input |
| TFPI_D[DB-1:0] | i | | | Data input |
| TFPI_RDY | i | | | Ready input |
| VG_TFPI_SEL_N | i | | | (Macro) select input (broadcast programming virtual global register) |
| TFPI_SEL_N | i | | | (Macro) select input (macro specific programming) |
| TR_TFPI_D[DB-1:0] | o | | | Data output |
| TR_TFPI_D_EN | o | | | Data enable (active high) |
| TFPI_RDY | o | | | Ready output |
| TR_TFPI_RDY_EN | o | | | Ready enable |

# 4 Register Description

## 4.1 Register Overview

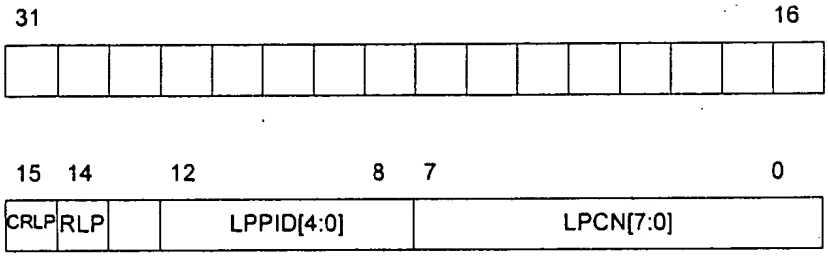
**Register Overview Table : TSAR V2.1**

| Register ID | Access | Absolute Address cs_n & a(7:2) | Reset Value | Comment |
|---|---|---|---|---|
| CONF2 | R/W | $44_H$ | $00000000_H$ | (virtual global) configuration register 2 |
| TSAIA | R/W | $70_H$ | $00000000_H$ | timeslot assignment indirect access register |
| TSAD | R/W | $74_H$ | $02000000_H$ | timeslot assignment data register |
| TAC | R/W | $58_H$ | $00000000_H$ | (virtual global) test command register |
| TD | R/W | $5C_H$ | $00000000_H$ | (virtual global) test data register |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

## 4.2 Detailed Register Description

## 4.3 (Virtual Global) Configuration Register 2 (CONF2)

Access : read/write
Address : $00000044_H$
Reset Value : $00000000_H$




*Note: This register is common for TSAT and other macros. The macro TSAT just collect those data bits from the written dword (see above), that are relevant for macro TSAT. With a read access to this register, the macro TSAT drive only a value for the relevant bits. All other bits are set to '0'.*

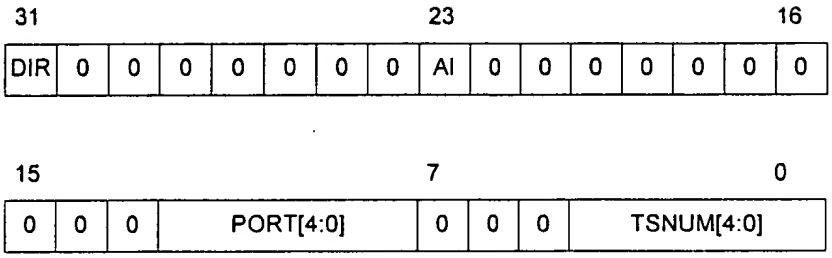
| | |
|---|---|
| LPCN[7:0]: | Channel selection for channelwise remote loop |
| LPPID[4:0]: | Port selection for portwise remote loop |
| CRLP: | '1'--> channelwise remote loop on channel selected by LPCN[7:0] |
| RLP: | '1' --> portwise remote loop on port selected by LPPID[4:0] |

### 4.3.1 Timeslot Assignment Indirect Access Register (TSAIA)

Access : read/write

Address : $00000070_H$

Reset Value : $00000000_H$




**Address:**

This register specifies the base address for access to the TARPT (TSAR parameter table RAM). The address is composed of timeslot number and port id. The address bit field TSNUM[4:0] corresponds to the timeslot number of port which is selected by the address bit field PORT[4:0].

| | |
|---|---|
| TSNUM[4:0] | timeslot number which is affected by access (T1 = 0..23, E1 = 0..31) |
| PORT[4:0] | port number which is affected by access (port 0..31) |

**DIR: transmit/receive direction**

1--> Timeslot Assigner Transmit

0--> Timeslot Assigner Receive

**AI: auto increment mode**

If set when writing a start address to the address pointer, the TSNUM bit field of the address will be automatically incremented (and wrapped at the maximum value x1F) after each read or write access to the data register.This simplifies the transfer of data blocks because the address register for a certain port has to be written only once at the beginning of a data transfer.

**Read access to TSAIA**

On read access to TSAIA TSAR responds, when DIR is set to '0' (which is the reset value). When DIR is set to '1' (which needs a write access first in order to set DIR) the TSAT should respond. The macro, which is not accessed, should respond with all '0'.

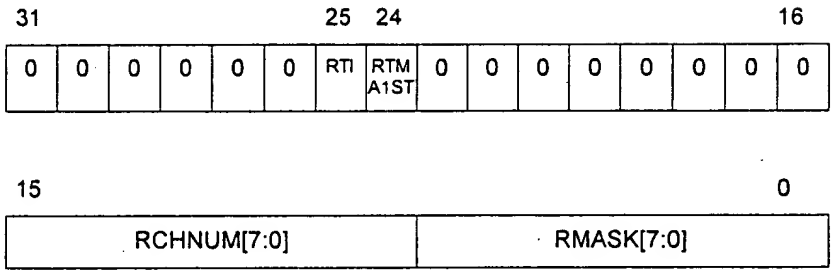
In case having used the autoincrement mechanism before, the returned value should be the actual address, i.e. the autoincremented timeslot number.

### 4.3.2 Timeslot Assignment Data Register (TSAD)

Access : write

Address : $00000074_H$

Reset Value : $02000000_H$




The data register is a port into the TARPT RAM for read and write access. The RAM address is specified by the address bit field in the timeslot assignment indirect access register. The TARPT RAM is initialized following hw_reset_n and sw_reset_n.

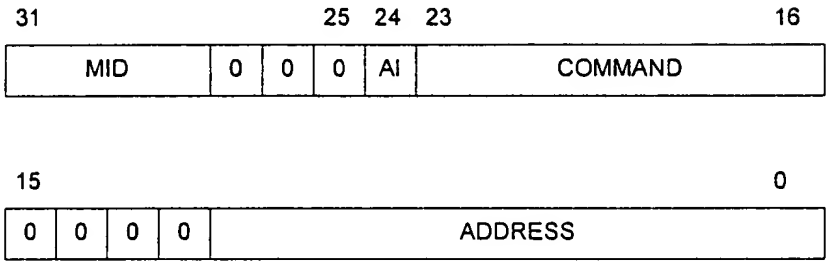
| | |
|---|---|
| RMASK[7:0] | receive mask bit field for bit rate adaption, mask bit = '1' bit is enabled, mask bit = '0' bit is discarded (reset value = $00_H$) |
| RCHNUM[7:0] | receive channel number, maps the corresponding timeslot to this logical channel (reset value = $00_H$) |
| RTMA1ST | receive TMA first (for TMA synchronisation purpose), TMA = '1' indicates first timeslot in a logical TMA channel (reset value = '0') |
| RTI | receive timeslot inhibit, RTI = '1' no request to the protocol machine for this timeslot, timeslot is discarded (reset value = '1') |

### 4.3.3 (Virtual Global) Test Command Register (TAC)

Access :read / write

Address : $00000058_H$

Reset Value : $00000000_H$




Refer to the Implementation Specification M256F for details to the TAC register.

MID: Macro ID Code (**TSAR: "0110"**)

AI: auto increment function

ADDRESS: internal address

CMD: command (select of RAM or register)

**CMD:**

Specifies the access to memory block or register being addressed. Defined command types are :

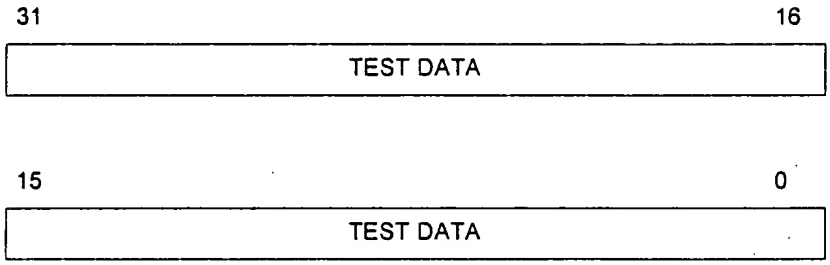
00000001 : TARPT testmode read (TSAR parameter table RAM)

10000001 : TARPT testmode write

On read access to TAC the macro which is selected via MID should respond to this access. All other macros should respond with all '0'.

### 4.3.4 (Virtual Global) Test Data Register (TD)

Access : read/write
Address : $0000005C_H$
Reset Value : $00000000_H$




Refer to the Implementation Specification M256F for details to the TD register.

The TD register is a port into theTARPT (TSAR parameter table RAM) for read and write access. The select of RAM and access type is specified by the command type bit field in the register TAC. The RAM address itself is specified by the address bit field in the register TAC.

**TARPT: TSA receive parameter table RAM**

TEST DATA[7:0]: receive mask bit field
TEST DATA[15:8]: receive channel number
TEST DATA[16]: receive TMA1ST flag
TEST DATA[17]: receive timeslot inhibit
TEST DATA[31:18]: '0'

## 5 Functional Test Specification (Macrolevel)

(use Checklist C06 "Function Checklist - Comparison of Specification vs. Circuit"
http://www.hl.siemens.de/lognet/hl_ta/dhb/f.htm)